IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

ANDREW M. WARWICK

Atty. Docket

GB 000029

Serial No.

Filed: CONCURRENTLY

TRENCH-GATE SEMICONDUCTOR DEVICES

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

7. (Amended) A semiconductor device as claimed in claim 1, wherein a patterned insulating layer is provided on the semiconductor body, wherein in the active cell area the insulating layer provides an insulating overlayer on the trench-gates and the insulating layer has windows where the source electrode contacts the source regions, and wherein in the inactive area a window in the insulating layer provides the gate electrode contact area.

8. (Amended) A semiconductor device as claimed in claim 1, wherein in the active cell area an insulating layer is provided in the trenches between the gate material in the trenches and the semiconductor body adjacent the trenches.

9. (Amended) A semiconductor device as claimed in claim 1, wherein the gate electrode provides a gate bond pad within the gate electrode contact area.

13. (Amended) A method as claimed in claim 10, further including the step of providing an insulating layer in the trenches in the active area and in the inactive area between the gate material in the trenches and the semiconductor body adjacent the trenches.

14. (Amended) A method as claimed in claim 10, further including the step of providing a gate bond pad with the gate electrode within the gate electrode contact area.

REMARKS

The claims have been amended in order to reformat the claims to delete all multiple dependencies prior to calculation of the filing fee and place the instant application in standard U.S. format.

Entry of this amendment prior to calculating the filing fee is respectfully requested.

Respectfully submitted,

By____________________
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March 13, 2001

APPENDIX

7. (Amended) A semiconductor device as claimed in claim 1 ~~any one of claims 1 to 6~~, wherein a patterned insulating layer is provided on the semiconductor body, wherein in the active cell area the insulating layer provides an insulating overlayer on the trench-gates and the insulating layer has windows where the source electrode contacts the source regions, and wherein in the inactive area a window in the insulating layer provides the gate electrode contact area.

8. (Amended) A semiconductor device as claimed in claim 1 ~~any preceding claim~~, wherein in the active cell area an insulating layer is provided in the trenches between the gate material in the trenches and the semiconductor body adjacent the trenches.

9. (Amended) A semiconductor device as claimed in claim 1 ~~any preceding claim~~, wherein the gate electrode provides a gate bond pad within the gate electrode contact area.

13. (Amended) A method as claimed in claim 10 ~~any one of claims 10 to 12~~, further including the step of providing an insulating layer in the trenches in the active area and in the inactive area between the gate material in the trenches and the semiconductor body adjacent the trenches.

14. (Amended) A method as claimed in claim 10 ~~any one of claims 10 to 13~~, further including the step of providing a gate bond pad with the gate electrode within the gate electrode contact area.